

G32A1465

Errata Sheet

Version: V 1.0

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1 Introduction

This document describes known limitations of the G32A1465 series products. If your application matches any scenario described in this errata sheet, use the recommended solution. If no solution is provided, avoid using the product in that scenario.

2 Errata List

Table 1 Errata List

Errata List	Introduction	产品版本
		A1
SYSMC	System hangs from asynchronous wakeup during VLPS entry.	√
	Invalid data may be read when accessing Flash in VLP mode.	√
CMU (Clock Management Unit)	Abnormal SCG system clock switching status.	√
	If HSI is disabled, the SCG clock controller may block the reset process.	√
CAN	Nominal-phase SJW incorrectly applied at the CRC delimiter.	√
	CODE field corruption when receive FIFO is used in classic CAN mode.	√

Note: √ indicates present, × indicates not present.

3 SYSMC System Mode Controller

3.1 System hangs from asynchronous wakeup during VLPS entry

Problem Description

If the bus clock equals the system clock and an asynchronous wakeup (such as an external interrupt) occurs while the system is switching from RUN to VLPS mode or from VLPR to VLPS mode, the system may enter an undefined state and hang. Recovery is possible only through a power reset or a watchdog reset.

Solution

Before entering VLPS mode, ensure that the system clock is at least twice the bus clock.

3.2 Invalid data may be read when accessing Flash in VLP mode

Problem Description

When the system is in VLP mode (VLPR or VLPS), and the system clock, core clock, and bus clock are all above 1 MHz, invalid data may be read if the CPU accesses Flash while the DMA also has a Flash transfer enabled, and both masters access PFlash and DFlash at the same time.

Solution

In VLPR or VLPS mode, software must ensure that all bus masters (CPU and DMA) access only PFlash or only DFlash at any given time. When switching from PFlash-only access to DFlash-only access, let the DMA task currently accessing PFlash finish, jump to an SRAM location, and wait 40 cycles to ensure the ongoing PFlash access is complete before accessing DFlash.

If simultaneous access to both PFlash and DFlash is truly required, run the system with the system clock, core clock, and bus clock all set to 1 MHz in LVP mode.

4 CMU Clock Management Unit

4.1 Abnormal SCG system clock switching status

Problem Description

When the system clock switches from one source to another, the SCG (System Clock Generator) status register SCG_CLKCFG[SYSCLKSSEL] may hold a corrupted value.

Solution

Have software read the same [SYSCLKSSEL] value twice in a row to confirm that the clock switch is complete.

4.2 If HSI is disabled, the SCG clock controller may block the reset process

Problem Description

If HSI is disabled (for example, SCG_HSIKSTS[HSIEN]=0), the device may enter a reset state and fail to operate normally when a reset type other than POR occurs.

Solution

Enable HSI by setting SCG_HSIKSTS[HSIEN] to 1.

If SCG_HSIKSTS[HSIEN] is disabled and a reset lockup occurs, perform a power restart to restore normal operation.

5 CAN

5.1 Nominal-phase SJW incorrectly applied at the CRC delimiter

Problem Description

When receiving a CAN-FD frame with Bit Rate Switch enabled, the synchronization jump width at the CRC delimiter incorrectly uses the arbitration-phase value, whereas the CAN specification requires the data-phase value.

Solution

No action is required. Because the CAN protocol is robust, the receiving node recovers automatically even if an incorrect synchronization jump width is applied.

5.2 CODE field corruption when receive FIFO is used in classic CAN mode

Problem Description

If the CODE field of a receive message buffer is corrupted, the buffer may be deactivated and unable to receive new messages. It may also be misinterpreted as another type of message buffer (for the receive buffer types, see the Message Buffer Structure section of the CAN chapter in the user manual).

The CODE field of a CAN receive message buffer (MB) may be corrupted if the following sequence occurs:

- (1) A message is received and transferred into an MB (for example, MBx).
- (2) A new message (for example, message1) begins to arrive, and serial message buffer 0 (SMB0) receives message1, which should belong to MBx.
- (3) Before SMB0 is moved to MBx, software locks MBx for more than 20 CAN bit times (this duration determines how likely the erratum is to appear). As a result, SMB0 is not transferred to MBx and continues to hold message1.
- (4) A later message (for example, message2) is loaded into SMB1 because SMB0 is full, and the CAN hardware evaluates it as belonging to the FIFO.
- (5) While message2 is being received, MBx is unlocked. SMB0 is then transferred to MBx, and the CODE field is updated with an incorrect value.

This problem does not occur if the application uses only the Rx FIFO or only dedicated MBs (that is, Rx MBs only or Rx FIFO only). It also does not occur when CAN FD (Flexible Data-rate CAN) is used. In short, it occurs only when the application configures CAN to receive using both the FIFO and dedicated MBs at the same time.

Solution

This defect occurs only when the receive FIFO is enabled. The FIFO is controlled by the FIFOEN bit in the module configuration register (MCFG). If the Rx FIFO is not used, the CODE field will not be corrupted.

The defect also does not occur if the receive buffer lock time is 20 CAN bit times or less.

After the hardware sets the interrupt flag for the corresponding MB (the MBx bit in the IFLG register), the CPU should read (process) the received frame using the following procedure:

- (1) Read the control and status word of the mailbox.
- (2) Check whether the BUSY bit (CODE[0]) is cleared to confirm that the mailbox is not locked.
If this bit is set, repeat step 1.
- (3) Read the contents of the mailbox.
- (4) Clear the corresponding flag bit in the IFLG register.
- (5) Read the free-running timer register (FRTMR) to unlock the mailbox.

To complete this procedure within 20 CAN bit times, run the MB receive handling routine (steps 1 through 5 above) as a critical section, with interrupts disabled beforehand, and ensure it completes within a deterministic number of cycles.

If the MB receive handling routine cannot be guaranteed to complete within 20 CAN bit times, do not combine the Rx FIFO with receive message buffers in classic CAN applications.

6 Revision History

Table 2 Document Revision History

Date	Version	Revision History
2026.7	1.0	● Initial release

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